7. (Amended) An integrated video display system for providing a video signal having reduced beat patterns, comprising:

a video data circuit coupled to an output circuit through a latching circuit, the video data circuit being configured to provide a video data signal based on a pixel frequency, the pixel frequency being based on an external clock reference; and

a re-clocking circuit coupled to the latching circuit, the re-clocking circuit being configured to provide a local clock signal for re-clocking the video data signal through the latching circuit, wherein re-clocking the circuit is based on the external clock reference, and the video data signal is provided to the output circuit based on the local clock signal.